Realization of Unidirectional Planar GaAs Nanowires on GaAs (110) Substrates

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***Abstract*—A self-aligned unidirectional planar GaAs nanowire (NW) array is realized by growing on (110) GaAs substrates through the Au-catalyzed vapor–liquid–solid mechanism. All NWs on (110) substrates propagate along the [00-1] direction, yielding planar NWs with trapezoidal cross sections where the top surface and sidewalls are identified by micro X-ray diffraction analysis to be [110], [010], and [100] facets, respectively. Depletion-mode long-channel metal–semiconductor field-effect transistors using these [00-1] GaAs NWs as channels exhibit well-defined dc output and transfer characteristics, confirming the high material quality of the NWs. Completely ordered site controlled arrays of planar NWs are demonstrated by growing on (110) substrates with Au catalyst nanoparticles patterned using electron beam lithography.**

***Index Terms*—GaAs, metal–semiconductor field-effect transistor (MESFET), nanowire (NW), nanowire array.**

I. Introduction

SEMICONDUCTOR nanowires (NWs) are becoming core nanotechnology building blocks for next-generation electronics [1], optoelectronics [2], nanoelectromechanical systems [3], and biological applications [4]. The ability to create ordered NW structures with controllability in size, orientation, position, and alignment is critical to future manufacturability and compatibility with existing semiconductor fabrication processes [5]. Growth via vapor–liquid–solid (VLS) mechanism is arguably the most commonly used method for the formation of single crystalline semiconductor NW structures including heterojunctions and p-n junctions in axial and radial directions.

However, most VLS NWs are grown vertically or out of plane with respect to their substrates. NWs grown in this fashion are prone to planar defects such as stacking faults and polytypic growth [6], which are problematic to device performance [7]. The out-of-plane orientation is also incompatible with traditional planar processes that are used in modern electronics. NWs usually have to be removed from the surface through external force and transferred to a new host substrate where the final device is fabricated [8]. Recently, our research group has reported a controlled method to grow Au-catalyzed VLS GaAs NWs in a planar orientation ⟨110⟩ epitaxially on GaAs (100) substrates [9], which are self-aligned and free of twin plane defects. Planar NW growth has also been reported on GaAs (311) substrates as well [10]. High-performance metal–semiconductor field-effect transistors (MESFETs) and high-electron-mobility transistors (HEMTs) have been demonstrated using these planar ⟨110⟩ GaAs NWs as the channels [11], [12]. However, on (100) substrates, self-aligned planar NWs propagate in either [01-1] or [0-11] direction, i.e. parallel or antiparallel as shown in Fig. 1(a) [9]. This is because these two orientations are crystallographically equivalent, which clearly prevents complete alignment through site control of the Au catalysts. The purpose of this work is to eliminate the antiparallel propagation direction and achieve completely ordered NW arrays as grown. We demonstrate that the choice of substrate orientation allows direct control of the available planar growth directions. We report the growth of unidirectional planar NWs, structural characterization, and MESFET device results using these NWs as the channel.

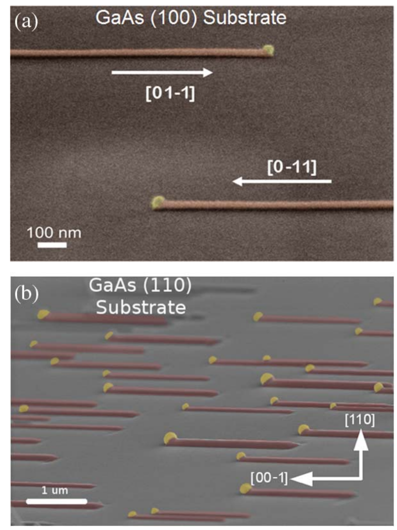

Fig. 1. SEM images (75° tilted and false colored) of self-aligned bidirectional and unidirectional planar NWs with the Au nanoparticles at the growth front. (a) Grown on a (100) substrate, with the planar NWs propagating randomly in either the [01-1] or the [0-11] direction as indicated. Adapted with permission from [9]. Copyright 2008 American Chemical Society. (b) Grown on a (110) substrate, with the planar NWs propagating unanimously in one single direction, [00-1].

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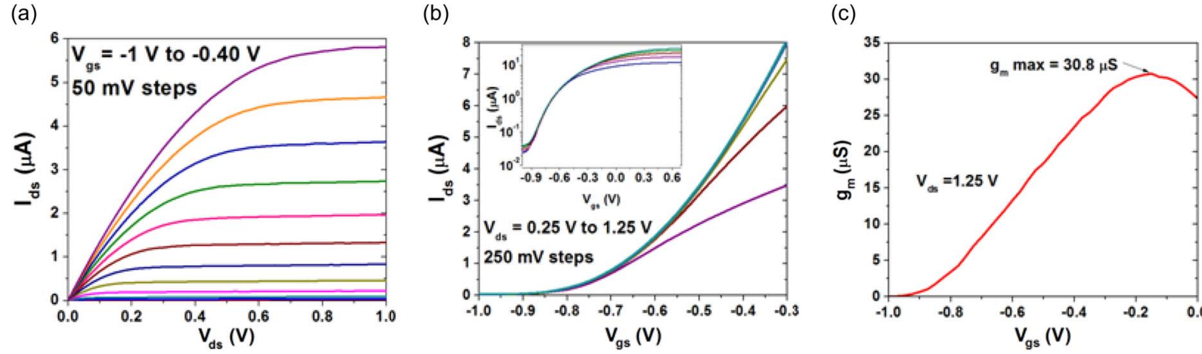

Fig. 2. DC output and transfer characteristics of a depletion-mode NW-MESFET using a [00-1] GaAs NW channel on a (110) GaAs substrate. (a) I_{ds} versus V_{ds} family of curves for V_{gs} from -1 to -0.4 V with 50-mV steps. (b) I_{ds} versus V_{gs} transfer characteristics for $V_{\mathrm{ds}} = 0.25$ to 1.25 V with 250-mV steps. The inset is I_{ds} versus V_{gs} on a semilog plot. (c) Transconductance g_m versus V_{gs} plot with maximum g_m of 30.8 μS (75.9 mS/mm when normalized to the NW base width).

II. Experimental

VLS planar GaAs NWs were grown using 250-nm colloidal gold (Au) nanoparticles as catalysts, and the growth was carried out in a horizontal-flow Aixtron metal organic chemical vapor deposition (MOCVD) reactor under atmospheric pressure. Epiready semi-insulating GaAs substrates of various orientations, including (100) and (110), were used for growth. For the growth of site-controlled NW arrays, a JEOL JBX-6000FS electron beam lithography system was used to pattern the GaAs substrates using PMMA resist, followed by the deposition of approximately 20 nm of Au thin film using an electron beam evaporator and then liftoff. To remove residual PMMA, the samples were exposed for 10 min to a 300-W O_2 plasma and then soaked in three different solvent baths consisting of acetone, methanol, and isopropanol for 10 min each. Arsine (AsH_3), trimethylgallium (TMGa), and disilane (Si_2H_6) were used as the arsenic (As), gallium (Ga), and silicon (Si, dopant) precursors, respectively. The desorption temperature in the MOCVD chamber was 625 °C, and the NW growth temperature was around 480 °C with a growth rate of $\sim$57 nm/s. MESFETs were fabricated using Ge/Au/Ni for the source and drain ohmic contact and Ti/Au for the top gate Schottky contact. The source-to-drain distance is $\sim$7 μm, and the gate length is 2 μm. More details of the device fabrication can be found elsewhere [11]. Postgrowth characterization was done with a Hitachi S-4800 field emission scanning electron microscope (SEM). Micro X-ray diffraction experiments using 10-keV synchrotron radiation were performed at the Sector 7 beamline of the Advanced Photon Source at Argonne National Laboratory. The X-ray beam was focused to an $\sim$20-μm spot size, with measurements performed in grazing incidence geometry to enhance surface sensitivity.

III. Results and Discussion

In typical out-of-plane epitaxial growth on GaAs (100) substrates, GaAs NWs have been shown to grow in the $\langle 111 \rangle B$ directions [13]. The NWs have equal chances to grow in either of the two $\langle 111 \rangle B$ directions: [1 1 $-$1] and [1 $-$1 1]. Under planar growth conditions on GaAs (100) substrates, GaAs NWs have equal chances to grow in the [0 1 $-$1] or [0 $-$1 1] crystal directions, parallel or antiparallel to each other [9], as shown in Fig. 1(a).

We have found that planar NWs tend to grow along the projections of $\langle 111 \rangle B$ crystal directions onto the substrate plane. Since there is only one $\langle 111 \rangle B$ direction on a (110) substrate, we are able to realize unidirectional planar NW growth using (110) substrates, as shown in Fig. 1(b). Through X-ray crystal truncation rod analysis of the facets' rods which originate at the 111 Bragg peak, the planar NWs are confirmed to grow unstrained and in full registry with the substrate in the [00-1] direction, with (100) and (010) side facets, i.e., a trapezoidal cross section with the (110) top facet parallel to the substrate surface and two $\langle 010 \rangle$ facets that form a 45° angle with the surface. The realization of completely parallel unidirectional planar NW growth has significant implications since it is now possible to make fully aligned arrays of NWs as will be demonstrated later.

Previously, we have reported device results of MESFETs [11] and HEMTs [12] using planar GaAs $\langle 110 \rangle$ NWs on semi-insulating GaAs (100) substrates as the channels. Here, we demonstrate MESFETs utilizing [00-1] planar NWs on a GaAs (110) substrate to prove their viability as a FET device channel. Fig. 2 shows the dc characteristics of a depletion-mode MESFET with an n-type Si-doped [00-1] planar NW as the channel. The family of $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ curves exhibits a linear region, onset of pinchoff, and saturation as shown in Fig. 2(a), indicating well-defined channel modulation behavior. The transfer characteristics $(I_{\mathrm{ds}} - V_{\mathrm{gs}})$ in Fig. 2(b) is shown for V_{ds} values in the range of 0.25 to 1.25 V, with the semilog plot of the same type shown in the inset. The $I_{\mathrm{on/off}}$ ratio of the device is $\sim$850. Further increase of $I_{\mathrm{on/off}}$ is expected with improved device isolation and reduction of parasitic deposition on the substrate. The subthreshold slope is 169 mV/dec, and the threshold voltage is -0.88 V taken at a V_{ds} of 100 mV. The maximum drive current $I_{\mathrm{ds}} - \max$ at a V_{gs} of 0.5 V is 96.3 $\mu\mathrm{A}/\mu\mathrm{m}$; the transconductance g_m is shown in Fig. 2(c) with maximum g_m at 30.8 μS or 75.9 mS/mm, where the base width of the NW (base, top, and height dimensions are 406, 126, and 140 nm, respectively) is used for dimension normalization. Dozens of devices were tested, and NWs of similar base widths showed comparable device performance. The dc characteristics of the [00-1] NW MESFET on (110) substrates

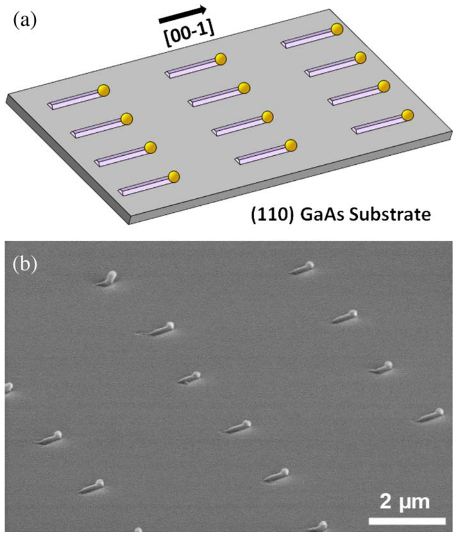

Fig. 3. (a) Illustration of site-controlled unidirectional planar NW array growth, with Au particles defined lithographically and growth taking place on a (110) substrate along [00-1] direction. (b) Tilted (75°) SEM micrograph of a completely ordered array of [00-1] GaAs NWs grown from E-beam patterned Au catalyst nanoparticles on a (110) GaAs substrate. The Au nanoparticle size is approximately 175 nm in diameter, and the NWs are $\sim$1.2 μm long.

demonstrated here are comparable to that of the control devices grown on (100) substrates, with slight enhancement as a result of improved fabrication. This confirms that [00-1] planar NWs grown on (110) substrates are just as viable as on (100) substrates for MESFET devices yet with better manufacturability for array-based channels as will be shown hereinafter.

The successful demonstration of high-quality unidirectional planar NW growth by using (110) substrates makes it possible to realize completely ordered NW arrays for array-based high-performance nanoelectronics. The ordering will be determined by the site control of the Au catalyst nanoparticles by lithographical patterning. One of the challenges of patterning is the introduction of organic contamination from the resist chemicals. NWs are known to be sensitive to contaminants during growth as the metallic nanoparticles can absorb precursors and impurities alike depending on their solid solubility. Impurities can dope the wire as well as cause abnormal growth to occur [14]. Planar NWs are extremely sensitive to impurities as they can not only infiltrate the catalyst nanoparticle but also contaminate the substrate surface that the epitaxial relationship of the entire NW sidewall is built on, preventing planar NW growth. Depending on the substrate treatment, we have observed NWs grown initially in the planar fashion but taking off from the surface to grow in out-of-plane mode soon after. Extensive substrate cleaning, including oxygen plasma and extended solvent soaks as described in the experimental section, is utilized to prevent NW growth deviating from the planar mode. Shown in Fig. 3 is an array of planar GaAs NWs on a (110) substrate successfully grown from Au catalyst nanoparticles patterned using electron beam lithography. It is evident that all the NWs unanimously propagated along the same direction, [00-1]. Devices using a completely ordered GaAs NW array will be reported separately.

IV. Conclusion

In summary, we have demonstrated the complete alignment of Au-catalyzed VLS planar GaAs NWs along the [00-1] crystal orientation by growing on (110) instead of (100) substrates. The unidirectional [00-1] NW-based long-channel MESFETs show excellent dc characteristics. With the inherent 3-D cross section, precise alignment and controlled placement through monolithic bottom–up growth demonstrated here, planar III–V NW array-based transistors could become a viable candidate for high-performance manufacturable bottom–up grown transistor technology beyond the Si roadmap.

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